CLAIMS

What is claimed is:

1. A method for performing an analysis of a network composed of at least one path, said method comprising:

generating a composite graph comprising K + 1 copies of an original graph, said original graph represents said network with zero defects and K is a predetermined maximum number of defects on any of said at least one path; and

performing an analysis of said network using said composite graph.

2. A method for performing fault tolerant static timing analysis for an electronic network composed of at least one path, said method comprising:

generating a composite timing graph comprising K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero defectsand K is a predetermined maximum number of defects present on any of said at least one path; and

performing a static timing analysis on said composite timing graph.

3. The method of claim 2, wherein

said network is composed of a plurality of nodes and each of said at least one path interconnects at least two of said plurality of nodes and

said performing static analysis further comprises calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal, and

at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

4. The method of claim 2, wherein said defects are due to one or more of the following:

manufacturing abnormalities insufficiently serious to cause a hard failure;

conductor coupling; and

voltage changes in floating components.

5. The method of claim 2, wherein K = 1, thereby resulting in a single-fault analysis.

6. The method of claim 2, wherein for each said i, where $0 \leqq i \leqq K$, a probability is associated with said condition of i defects in said path.

7. The method of claim 2, wherein said copies j, where 1 <= j <= K, of said original timing graph include only a preselected portion of said network preselected as being susceptible to defects.

8. The method of claim 7, wherein said original timing graph includes only a preselected portion of said network preselected as being susceptible to defects.

9. A method for performing K-fault tolerant static timing analysis for an electronic network composed of at least two nodes and at least one path interconnecting said nodes, said method comprising:

generating an original timing graph for said network, said original timing graph having at least one delay edge E, each said delay edge E having a source node and a sink node;

generating a composite timing graph including K + 1 copies of said original timing graph, where K is a predetermined maximum number of defects of a first type on any of said at least one path;

adding a first type of defect edge for at least K of said delay edge E in said original timing graph, such that each said first type of defect edge has a delay that reflects a timing behavior of the circuit in a presence of a first type of defect from said source node of E in $copy_i$ of said timing graph to said sink node of E in $copy_{i+1}$ of the said composite timing graph, for all values of i such that 0 <= i < K; and

for each said node, calculating at least one parameter.

10. The method of claim 9, wherein said at least one parameter comprises at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal, and

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

11. A method for performing K-fault tolerant static timing analysis for an electronic network composed of at least one path, said method comprising:

creating an original empty array representing a timing graph of said network with zero defects;

augmenting said original empty array to create an array representing K+1 copies of said timing graph, wherein K is a predetermined maximum number of defects present on any of said at least one path; and

performing a static timing analysis to fill in values for said augmented array.

12. The method of claim 11, wherein said network is composed of a plurality of nodes and each of said at least one path interconnects at least two of said plurality of nodes and wherein said performing static timing analysis further comprises:

calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of said signal,

at least one required arrival time (RAT) for said signal, and

an at least one slack value for said signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

13. A method within a data processing system for performing K-fault tolerant static timing analysis for a network composed of at least one path, each said path including at least two nodes, said method comprising:

generating a composite timing graph representing K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero defects and K is a predetermined maximum number of defects present on any of said at least one path; and

performing a static timing analysis on said composite timing graph by calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal, ~~and~~

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

14. A computer-readable medium containing a set of instructions for performing K-fault tolerant static timing analysis for a network composed of at least one path, each said path including at least two nodes, said instructions comprising:

generating a composite timing graph representing K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero defects and K is a predetermined maximum number of defects present on any of said at least one path; and

performing a static timing analysis on said composite timing graph by calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal,

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

15. A system containing a set of instructions for performing K-fault tolerant static timing analysis for a network composed of at least one path, each said path including at least two nodes, said instructions comprising:

generating a composite timing graph representing K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero defects and K is a predetermined maximum number of defects present on any of said at least one path; and

performing a static timing analysis on said composite timing graph by calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal,

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

16. A system for performing K-fault tolerant static timing analysis for a network composed of at least one path, each said path including at least two nodes, said system comprising:

means for generating a composite timing graph representing K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero defects and K is a predetermined maximum number of defects present on any of said at least one path; and

means for performing a static timing analysis on said composite timing graph by calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal,

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

17. An apparatus for performing K-fault tolerant static timing analysis for a network composed of at least one path, each said path including at least two nodes, said apparatus comprising:

a control unit; and

a memory unit, wherein

said control unit generates in said memory unit a composite timing graph representing K + 1 copies of an original timing graph, said original timing graph represents a timing graph of said network with zero defects and K is a predetermined maximum number of defects present on any of said at least one path; and said control unit further performs a static timing analysis on said composite timing graph by calculating, for each said node in each said path, at least one of the following:

at least one arrival time (AT) of an input signal,

at least one required arrival time (RAT) for said input signal, and

an at least one slack value for said input signal, wherein each said slack value is a difference between said at least one RAT and said at least one AT.

18. A method for performing a delay tolerance static timing analysis for infrequently occurring coupling delays between adjacent simultaneously-transitioning conductors in an electronic network composed of at least one path, said method comprising:

generating a composite timing graph comprising K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with zero coupling delays and K is a predetermined maximum number of coupling delays present on any of said at least one path; and

performing a static timing analysis on said composite timing graph.

19. A method for performing a delay tolerance static timing analysis for circuit element delay variations having a bimodal distribution in an electronic network composed of at least one path, said method comprising:

generating a composite timing graph comprising K + 1 copies of an original timing graph, wherein said original timing graph represents a timing graph of said network with delays from a first mode of said bimodal delay distribution and K is a predetermined maximum number of delays from a second mode of said bimodal delay distribution present on any of said at least one path; and

performing a static timing analysis on said composite timing graph.

20. The method of claim 9 where said original timing graph includes at least one test edge between a pair of nodes, and where a copy of said test edge is inserted between said endpoints of the said test edge in all pairs $copy_i$ and $copy_j$ of said original timing graph such that $i + j = K$.

21. The method of claim 20 where a defect test edge representing the behavior of the circuit in the presence of a first type of defect on said test edge, is inserted between said endpoints of the said test edge in all pairs $copy_r$ and $copy_s$ of said original timing graph such that $r + s + 1 = K$.

22. The method of claim 9 where a second type of defect edge is inserted between said source node of E in $copy_i$ of said timing graph to said sink node of E in $copy_{i+v}$ of the said composite timing graph, for all values of i such that $0 <= i <= K - v$ and $v > 1$, said second type of defect edge representing the behavior of the circuit in the presence of a second type of defect on edge E, said second type of defect being of lower probability than said first type of defect; and

for each said node, calculating at least one parameter.